



(An Autonomous Institution - AFFILIATED TO ANNA UNIVERSITY, CHENNAI)

S.P.G.Chidambara Nadar - C.Nagammal Campus

S.P.G.C. Nagar, K.Vellakulam – 625 701 (Near VIRUDHUNAGAR).

Department of Electronics and Communication Engineering

Course Code	Course Name	L	T	P	C
Value Added Course	HARDWARE DESIGN USING SYSTEM VERILOG	20	0	25	2

a. Preamble

Digital systems form the backbone of nearly every modern electronic device, from smartphones to automotive control units. As the semiconductor and VLSI industry continues to grow, there is an increasing demand for engineers who can design, model, and verify digital circuits using industry-standard Hardware Description Languages (HDLs). This Value-Added Course on "Hardware Design using System Verilog" is designed to introduce students to the fundamentals of System Verilog and its application in designing combinational and sequential digital circuits.

b. Course Outcome

Upon successful completion of the course, the students will be able to

Cos	Course Outcome	Knowledge Level
CO1	Apply the fundamentals of SystemVerilog syntax, data types, and operators to write and simulate simple HDL programs using the EDA Playground environment.	K3
CO2	Apply combinational logic design concepts to construct and simulate basic digital circuits such as adders, multiplexers, decoders, and comparators using SystemVerilog.	K3
CO3	Apply testbench development techniques to generate stimulus, verify functional correctness, and interpret simulation waveforms for a given digital design.	K3
CO4	Apply sequential circuit design principles to implement and simulate flip-flops, counters, and registers using SystemVerilog constructs.	K3
CO5	Apply the concepts of finite state machines and modular design to build and simulate a complete digital sub-system as part of a mini project.	K3

Unit 1- Introduction to SystemVerilog:**7 Hours**

HDL overview; why SystemVerilog; digital design flow (RTL → Simulation → Synthesis), Data types: logic, bit, reg, wire, int; vectors and bit-widths Number representation (binary, hex, decimal); constants and parameters, Operators: arithmetic, relational, logical, bitwise, reduction, shift, concatenation, replication

Hands-on: Run sample code; write basic modules using different data types/operators; use \$display.

Unit 2- Combinational Circuit Design:**7 Hours**

Combinational logic basics; truth table to logic, assign statements and continuous assignment; conditional operator, always_comb block; if-else and case statements, Basic gates, Half Adder, Full Adder, Multiplexer (2:1, 4:1), Decoder (2:4), Encoder/Priority Encoder, Comparator

Hands-on: Design and simulate Full Adder, MUX, Decoder, Comparator.

Unit 3- Testbenches & Verification Basics:**7 Hours**

Concept of DUT; why testbenches are needed, Module instantiation (positional & named port mapping), Stimulus generation: initial block, #delay, Displaying/checking results: \$display, \$monitor, self-checking logic with if. Reading and interpreting waveforms in EPWave

Hands-on: Write a self-checking testbench for the Full Adder/MUX designed in Module 2.

Unit 4- Sequential Circuit Design – Flip-Flops & Counters:**7 Hours**

Combinational vs sequential circuits; clocks and edge-triggering (posedge/negedge), always_ff block; blocking (=) vs non-blocking (<=) assignment, D Latch, D Flip-Flop, JK Flip-Flop, T Flip-Flop, Synchronous/asynchronous reset; Up/Down Counters, Modulo-N counters.

Hands-on: Design and simulate D Flip-Flop, JK Flip-Flop, and a 4-bit up-down counter with reset.

Unit 5- Registers, FSM & Mini Project:**7 Hours**

Shift registers: SISO, SIPO, PISO, PIPO, FSM basics: Moore vs Mealy; enum for state encoding, Simple FSM example: sequence detector (e.g., detect "101"), Debugging tips using waveforms; coding best practices,

Mini project**(10 Hours)**

SDG Mapping

CO's	SDG Mapping			
CO1	SDG – 04 Quality Education	SDG – 09 Industry, Innovation and Infrastructure	–	–
CO2	SDG – 04 Quality Education	SDG – 09 Industry, Innovation and Infrastructure	SDG – 12 Responsible Consumption and Production	–
CO3	SDG – 04 Quality Education	SDG – 09 Industry, Innovation and Infrastructure	SDG – 08 Decent Work and Economic Growth	–
CO4	SDG – 04 Quality Education	SDG – 09 Industry, Innovation and Infrastructure		–
CO5	SDG – 04 Quality Education	SDG – 09 Industry, Innovation and Infrastructure		SDG – 08 Decent Work and Economic Growth

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6/7/24

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